ABSTRACT

A boosting circuit is disclosed. The boosting circuit comprises a reference voltage generating circuit unit for generating a reference voltage according to an address transition detection signal that is delayed by a given time, a first boosting means for outputting a given boosting voltage according to the address transition detection signal and an inverted signal thereof, a sensing circuit for sensing a flash memory cell according to the reference voltage and the boosting voltage of the first boosting means, wherein the output signal of the sensing circuit is changed depending on the boosting voltage of the first boosting means applied to a gate terminal of the flash memory cell, a switching circuit for applying the boosting voltage of the first boosting circuit or the power supply voltage depending on the boosting voltage of the first boosting circuit and the output signal of the sensing circuit, and a second boosting means for supplying the power supply voltage to an output terminal according to the address transition detection signal, wherein the second boosting means is boosted according to the boosting voltage of the first boosting circuit or the power supply voltage to output the boosting voltages of two levels to the output terminal. Therefore, it is possible to prevent stress from being applied to the word lines of the cell due to a high voltage applied to the word lines, prevent unnecessary consumption of current and secure the read-out margin.